REMARKS

This responds to the Office Action dated March 22, 2006. Claims 1-31 are pending in this application.

§*102 Rejection of the Claims*

Claims 1-3 and 14 were rejected under 35 USC § 102(b) as being anticipated by Fiedler (U.S. 5,726,588). Applicant respectfully traverses the rejection. The Office Action fails to establish a *prima facie* case of anticipation because Fiedler does not teach or suggest all of the elements recited or incorporated into the claims.

Regarding claims 1-3:

Applicant cannot find in Fiedler any teaching or suggestion of, among other things, an apparatus comprising,

> a first differential output driver to provide a single ended output voltage in response to an input voltage; and a second differential output driver to provide a single ended output in response to the input voltage,

as recited or incorporated into claims 1-3. Fiedler says that a differential-to-CMOS level converter 10 is a balanced comparator with differential inputs 12a and 12b and complementary outputs 14a and 14b.[1] Thus, Fiedler only refers to one differential circuit. The Office Action reads transistors M1 and M2 of FIG. 1 of Fiedler onto the first and second differential out drivers recited in claim 1.[2] However, Fiedler refers to transistors M1 and M2 which form a [single] differential transistor pair.[3]

Fiedler also says that differential-to-CMOS level converters are commonly implemented on integrated circuits, such as application specific integrated circuits (ASIC) using complementary metal-oxide semiconductor (CMOS) technology, and that it is desirable to implement certain circuit functions with differential logic to rail-to-rail CMOS levels.[4] Thus Fiedler does not refer to an output driver but to a level converter on an integrated circuit. The

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[1] Fiedler, col. 2 lines 64-66.
[2] Office Action, pg.2.
[3] Fiedler, col. 3 lines 1 and 2.
[4] Fiedler, col. 1 lines 17-25.

Office Action itself characterizes the converter circuit 32 of Fiedler as a differential receiver[5] rather than a output driver.

> Additionally, Applicant cannot find any disclosure of,
>
> a feedback circuit to monitor the first and second output voltages and apply a bias voltage to at least one of the first and second output drivers,

as recited in claim 1. Fiedler refers to where a cross-over voltage adjustment circuit 36 monitors the cross-over voltage of the signals on circuit nodes N8 and $\overline{N8}$, compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$, in response to the comparison.[6] Thus, Fiedler does not describe the feedback structure recited in claim 1.

Further, in regard to claim 3, Applicant can find no disclosure in the cited portions of Fiedler to positive and negative conductors of a transmission cable, as recited in the claim 3.

Regarding claim 14:

Applicant cannot find in Fiedler any teaching or suggestion of, among other things, a method comprising,

> providing a correcting bias voltage proportional to a difference between the cross-over voltage and the equidistant voltage, and applying the correcting bias voltage to the differential drivers to vary the voltage point where the first and second output voltages cross-over,

as recited in claim 14. Instead, Fiedler compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$ in response to the comparison[7] instead of applying a correcting bias voltage to differential drivers.[8]

Applicant respectfully requests reconsideration and allowance of claims 1-3 and 14.

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[5] Office Action, pg. 7 middle paragraph.
[6] Fiedler, col. 4 lines 11-15.
[7] Fiedler, col. 4 lines 11-15.
[8] Id.

§103 Rejection of the Claims

1. Claims 4-12 and 15-24 were rejected under 35 USC § 103(a) as being unpatentable over Fiedler. (The Office Action stated that the claims are rejected as applied to claim 5 above. Applicant is proceeding under the assumption that it was intended to refer to claim 1 in the rejection.) Applicant respectfully traverses the rejection. The Office Action fails to establish a *prima facie* case of obviousness because Fiedler does not teach or suggest all of the elements recited or incorporated into the claims.

Claims 4-12 ultimately depend on base claim 1 and claims 15-24 ultimately depend on base claim 14. As set forth above, Applicant believes base claims 1 and 14 to be allowable at least for the reason that Fiedler does not teach or suggest all of the elements of the base claims.

Additionally, regarding claim 9, Applicant cannot find in Fiedler, among other things, any teaching or suggestion of an apparatus comprising,

> a differential receiver ... having a first output; a single-ended receiver ... having a second output; and a single-ended receiver ... having a third output; and wherein if the cross-over voltage is lower than the equidistant voltage, charge on the first capacitor is reduced while the first output is high and the second output is low and/or charge on the second capacitor is reduced while the first output is low and the third output is low;

as recited in claim 9. The Office Action asserts that single ended receivers for detecting rail-to-rail transitions are found in FIG. 2 of Fiedler. However, Fiedler relates that FIG. 2 is a schematic diagram of a differential-to-CMOS level converter;[9] so Fiedler does not teach or suggest single ended receivers. Also, Applicant cannot find where the charge placed on a capacitor is reduced based on output states of a differential and single ended receiver as recited in claim 9. Instead, Fiedler compares the cross-over voltage to a reference voltage, and sources or sinks equal offset currents into or from circuit nodes N6 and $\overline{N6}$ in response to the comparison[10]

Further regarding claim 22, Applicant cannot find in Fiedler any teaching or suggestion of a method comprising,

> measuring a cross-over transition on positive and negative conductors ... measuring a rail-to-rail transition on the positive conductor ... and measuring a rail-to-rail transition on the negative conductor ... and wherein producing a net

[9] Fiedler, col. 3 lines 43-44.
[10] Fiedler, col. 4 lines 11-15.

> charge includes switching a charge onto the capacitor when there is a mismatch in transition times,

as recited in claim 22. Instead, Fiedler refers to a comparison of the cross-over voltage to a reference voltage,[11] rather than a mismatch in transition times.

Applicant respectfully requests reconsideration and allowance of claims 4-12 and 15-24.

2. Claim 13 was rejected under 35 USC § 103(a) as being unpatentable over the combination of Haq (U.S. 6,430,606 B1) and Fiedler as applied to claim 1 above, and further in view of Varma et al. (U.S. 6,946,904 B1). Applicant respectfully traverses the rejection.

Claim 13 depends on base claim 1. As set forth above, Applicant believes that base claim 1 is allowable at least for the reason that Fiedler does not teach or suggest all of the elements of the base claim. The addition of Haq and Varma fail to provide the missing elements. Applicant respectfully requests reconsideration and allowance of claim 13.

3. Claims 25-31 were rejected under 35 USC § 103(a) as being unpatentable over Haq (U.S. 6,430,606 B1) in view of Fiedler (U.S. 5,726,588). Applicant respectfully traverses the rejection. The Office Action fails to establish a *prima facie* case of obviousness because proper motivation is lacking to combine Haq with Fiedler.

Fiedler relates to a differential-to-CMOS level converter.[12] Haq refers to a master 205 configured to communicate twenty signals including single ended-signals S0-S17 and small-swing complementary-source synchronous voltage and timing references SSVTR and /SSVTR.[13] Haq also refers to where a slave 210 may include multiple receivers (405 in FIG. 4) wherein each receiver 405 includes two comparators, one for comparing the signal against SSVTR and the other for comparing the signal against /SSVTR.[14] Thus, Haq does not disclose receiving SSVTR and /SSVTR differentially, but receives single ended signals with SSVTR or /SSVTR. Therefore, Haq does not describe a cross-over voltage on a differential communication bus. Haq also refers to high frequency signaling requiring small signal amplitudes to consume reasonable

[11] Fiedler, col. 4 lines 11-15.
[12] Fiedler, Abstract.
[13] Haq, col. 6 lines 31-35.
[14] Haq, col. 6 lines 45-49.

power,[15] such as 0.5v.[16] Thus, one of ordinary skill in the art would not be lead to combine Haq with a device using the CMOS levels in Fiedler to drive signals on a communication bus.

Additionally, Haq refers to where the system and method advantageously eliminate the need for a high-impedance VREF signal for comparison of small-swing single-ended signals.[17] Haq also explicitly states that there is no VREF (reference voltage) for comparison with the signal voltage,[18] and lists advantages of doing so.[19] Fiedler relies on comparing the cross-over voltage to a reference voltage.[20] Thus, Haq teaches away from the voltage reference comparison of Fiedler and one of ordinary skill in the art would not be lead to combine Haq with Fiedler.

Applicant respectfully requests reconsideration and allowance of claims 25-31.

[15] Haq, col. 1 lines 45-46.
[16] Haq, col. 9 lines 15-18.
[17] Haq, col. 3, lines 40-47
[18] Haq, col. 12, lines 45-50.
[19] Haq, col. 1 lines 53-55, col. 3 lines 42-47, and col. 12 lines 45-50.
[20] Fiedler, col. 4 lines 11-15.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-371-2172) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

JAMES D. PATTERSON

By their Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
612-371-2172

Date June 22, 2006 By Paul J. Urbanski
Paul J. Urbanski
Reg. No. 58,351

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of June, 2006.

Amy Moriarty
Name

Signature